**Homework 4**

**Part 1**

**Question 1: Design an 8 *−* 4 *−* 2 *−* 1 BCD code convertor to drive the seven-segment indicator in Fig. 1.**

1. **Build the truth table of your seven-segment display module.**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | X1 | X2 | X3 | X4 | X5 | X6 | X7 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | x | x | x | x | x | x | x |
| 1 | 0 | 1 | 1 | x | x | x | x | x | x | x |
| 1 | 1 | 0 | 0 | x | x | x | x | x | x | x |
| 1 | 1 | 0 | 1 | x | x | x | x | x | x | x |
| 1 | 1 | 1 | 0 | x | x | x | x | x | x | x |
| 1 | 1 | 1 | 1 | x | x | x | x | x | x | x |

1. **Using K-maps, find the minimum SOP expression for *X*1*, X*2*, X*3*, X*4*, X*5*, X*6*,* and *X*7 shown in Fig. 1.**

X1 (A, B, C, D) = ∑m (0, 2, 3, 5, 7, 8, 9)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 0 | 0 1 | 1 3 | 1 2 |
| 01 | 0 4 | 1 5 | 1 7 | 0 6 |
| 11 | x 12 | x 13 | x 15 | x 14 |
| 10 | 1 8 | 1 9 | x 11 | x 10 |

X1 (A, B, C, D) =A+B’C+BD+B’D’

X2 (A, B, C, D) = ∑m (0, 1, 2, 3, 4, 7, 8, 9)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 0 | 1 1 | 1 3 | 1 2 |
| 01 | 1 4 | 0 5 | 1 7 | 0 6 |
| 11 | x 12 | x 13 | x 15 | x 14 |
| 10 | 1 8 | 1 9 | x 11 | x 10 |

X2 (A, B, C, D) =B’+CD+C’D’

X3 (A, B, C, D) = ∑m (0, 1, 3, 4, 5, 6, 7, 8, 9)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 0 | 1 1 | 1 3 | 0 2 |
| 01 | 1 4 | 1 5 | 1 7 | 1 6 |
| 11 | x 12 | x 13 | x 15 | x 14 |
| 10 | 1 8 | 1 9 | x 11 | x 10 |

X3 (A, B, C, D) =C’+D+B

X4 (A, B, C, D) = ∑m (0, 2, 3, 5, 6, 8)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 0 | 0 1 | 1 3 | 1 2 |
| 01 | 0 4 | 1 5 | 0 7 | 1 6 |
| 11 | x 12 | x 13 | x 15 | x 14 |
| 10 | 1 8 | 0 9 | x 11 | x 10 |

X4 (A, B, C, D) =B’D’+B’C+CD’+BC’D

X5 (A, B, C, D) = ∑m (0, 2, 6, 8)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 0 | 0 1 | 0 3 | 1 2 |
| 01 | 0 4 | 0 5 | 0 7 | 1 6 |
| 11 | x 12 | x 13 | x 15 | x 14 |
| 10 | 1 8 | 0 9 | x 11 | x 10 |

X5 (A, B, C, D) =B’D’+CD’

X6 (A, B, C, D) = ∑m (0, 4, 5, 6, 8, 9)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 0 | 0 1 | 0 3 | 0 2 |
| 01 | 1 4 | 1 5 | 0 7 | 1 6 |
| 11 | x 12 | x 13 | x 15 | x 14 |
| 10 | 1 8 | 1 9 | x 11 | x 10 |

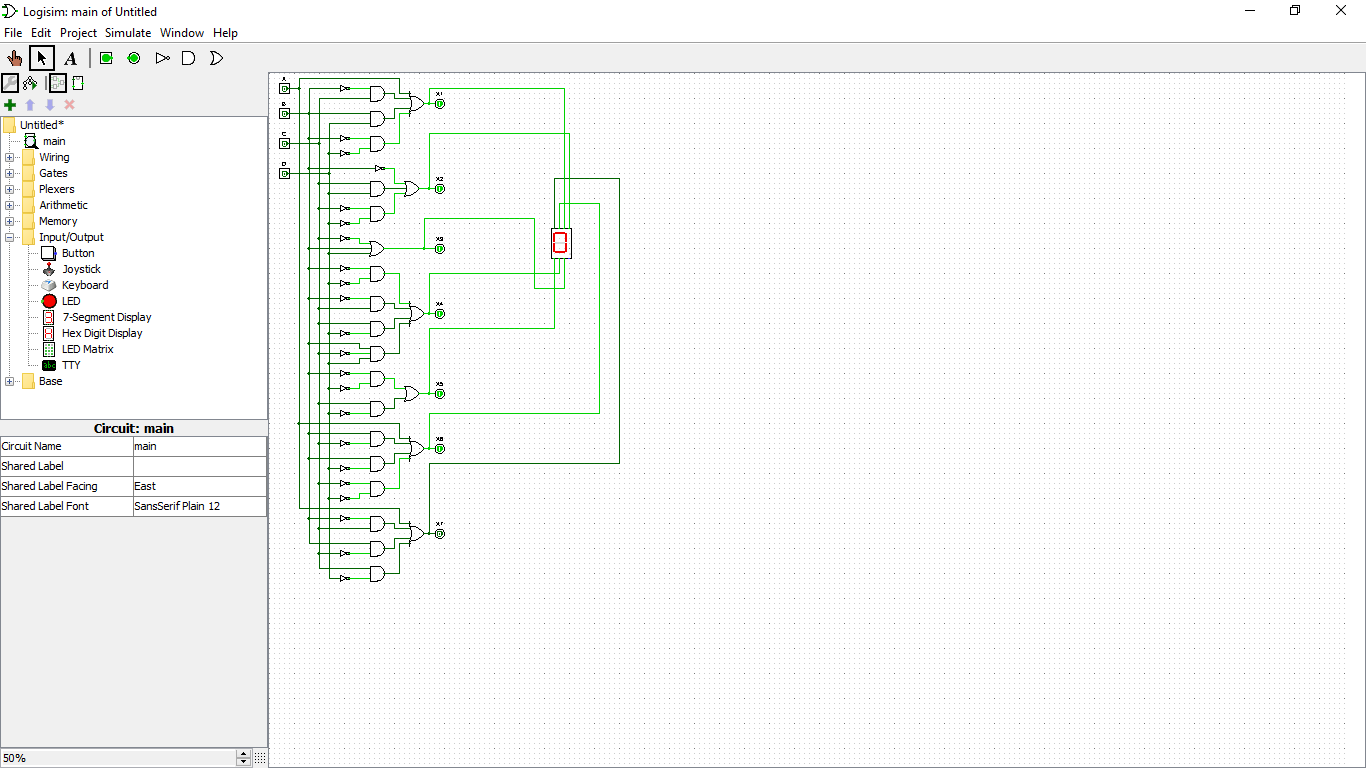
X6 (A, B, C, D) =A+BC’+BD’+C’D’

X7 (A, B, C, D) = ∑m (2, 3, 4, 5, 6, 8, 9)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 0 0 | 0 1 | 1 3 | 1 2 |
| 01 | 1 4 | 1 5 | 0 7 | 1 6 |
| 11 | x 12 | x 13 | x 15 | x 14 |
| 10 | 1 8 | 1 9 | x 11 | x 10 |

X7 (A, B, C, D) =A+B’C+BC’+CD’

1. **Plot the logic circuit of your seven-segment display module.**



**Part 2**

**Question 1: Show how a full adder (FA) can be constructed from HAs (provide a logic diagram for your solution)**

A  
B  
Cin

FA

S

Cout

A XOR B XOR Cin

AB+ACin+BCin

HA1

HA2

A

B

S1

Cout1

S2

Cout2

+

A XOR B XOR Cin

Cin(A XOR B)

AB+Cin(A XOR B)

Cin

AB+Cin(A XOR B)

=AB+Cin(A’B+AB’)  
=AB+A’BCin+AB’Cin

=A(B+B’Cin)+A’BCin   
=A(B+Cin)+A’BCin  
=AB+ACin+A’BCin  
=B(A+A’Cin)+ACin  
=AB+BCin+ACin **using Distributive and Absorptive laws**

**Question 2: Design a half subtracter (HS) that has two input bits *X* and *Y*, and two output bits *D* and *B*, where *D* is the difference between *X* and *Y*, and *B* is the borrow signal.**

1. **Provide a truth table of the half subtracter.**

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | D | B |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

1. **Provide a Boolean expression for each output, and use Karnaugh maps to simplify each output.**

D(X,Y)=X XOR Y

|  |  |  |
| --- | --- | --- |
| X\Y | 0 | 1 |
| 0 | 0 0 | 1 1 |
| 1 | 1 2 | 0 3 |

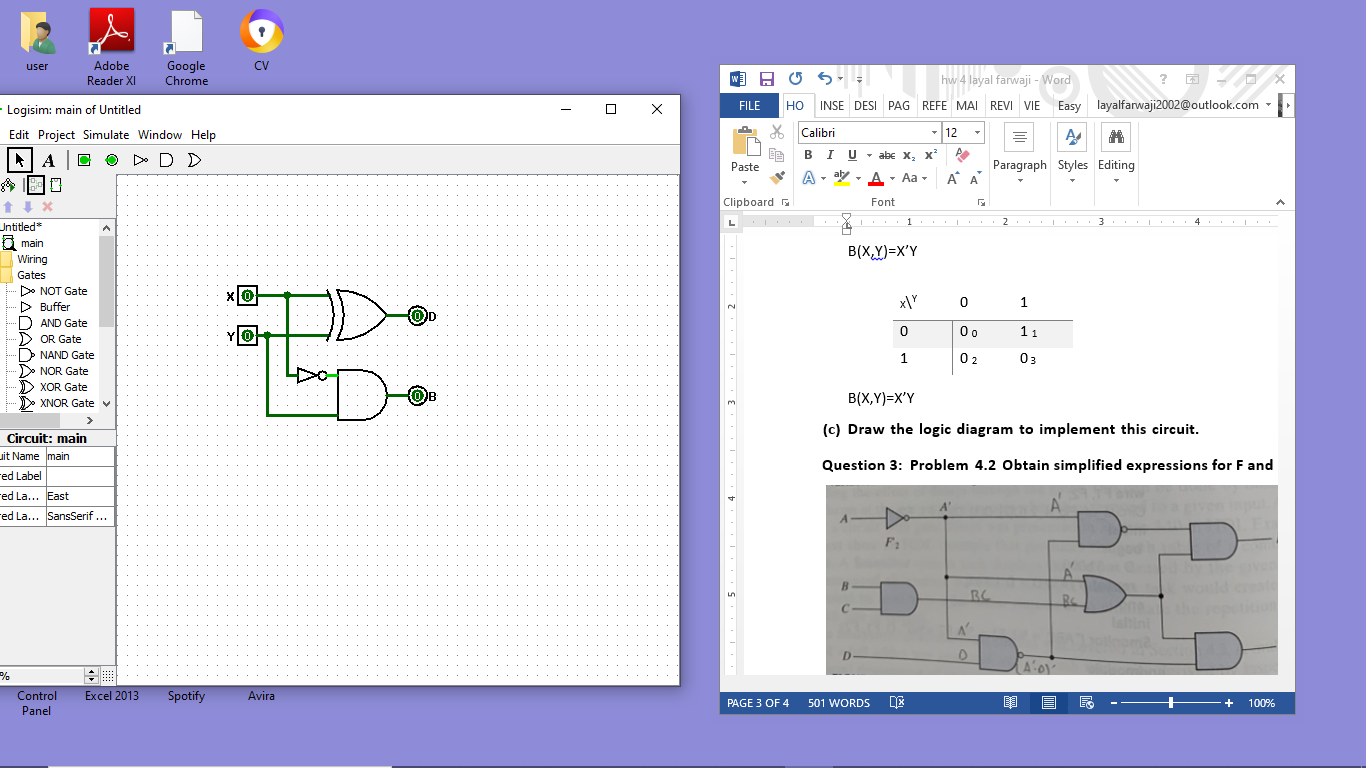
D(X,Y)=X’Y+XY’

B(X,Y)=X’Y

|  |  |  |
| --- | --- | --- |
| X\Y | 0 | 1 |
| 0 | 0 0 | 1 1 |
| 1 | 0 2 | 0 3 |

B(X,Y)=X’Y

1. **Draw the logic diagram to implement this circuit.**



**Question 3: Problem 4.2 Obtain simplified expressions for F and G using K-maps**

F(A,B,C,D)=(A’(A’D)’)’(A’+BC)  
=(A+A’D)(A’+BC)  
=AA’+ABC+A’A’D+A’BCD  
=ABC+A’D+A’BCD  
=ABC(D+D’)+A’D(B+B’)(C+C’)+A’BCD  
=ABCD+ABCD’+A’BCD+A’BC’D+A’B’CD+A’B’C’D+A’BCD  
=ABCD+ABCD’+A’BCD+A’BC’D+A’B’CD+A’B’C’D **using Complement, Distributive and Idempotent laws**F(A,B,C,D)=∑m(1,3,5,7,14,15)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 0 0 | 1 1 | 1 3 | 0 2 |
| 01 | 0 4 | 1 5 | 1 7 | 0 6 |
| 11 | 0 12 | 0 13 | 1 15 | 1 14 |
| 10 | 0 8 | 0 9 | 0 11 | 0 10 |

F(A,B,C,D)=A’D+ABC  
  
G(A,B,C,D)=(A’+BC)(A’D)’  
=(A’+BC)(A+D’)  
=AA’+A’D’+ABC+BCD’  
=A’D’+ABC+BCD’  
=A’D’(B+B’)(C+C’)+ABC(D+D’)+BCD’(A+A’)  
=A’BCD’+A’BC’D’+A’B’CD’+A’B’C’D’+ABCD+ABCD’+ABCD’+A’BCD’  
=A’BCD’+A’BC’D’+A’B’CD’+A’B’C’D’+ABCD+ABCD’ **using Complement, Distributive and Idempotent laws**

G(A,B,C,D)=∑m(0,2,4,14,15)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 0 | 0 1 | 0 3 | 1 2 |
| 01 | 1 4 | 0 5 | 0 7 | 1 6 |
| 11 | 0 12 | 0 13 | 1 15 | 1 14 |
| 10 | 0 8 | 0 9 | 0 11 | 0 10 |

G(A,B,C,D)=A’D’+ABC

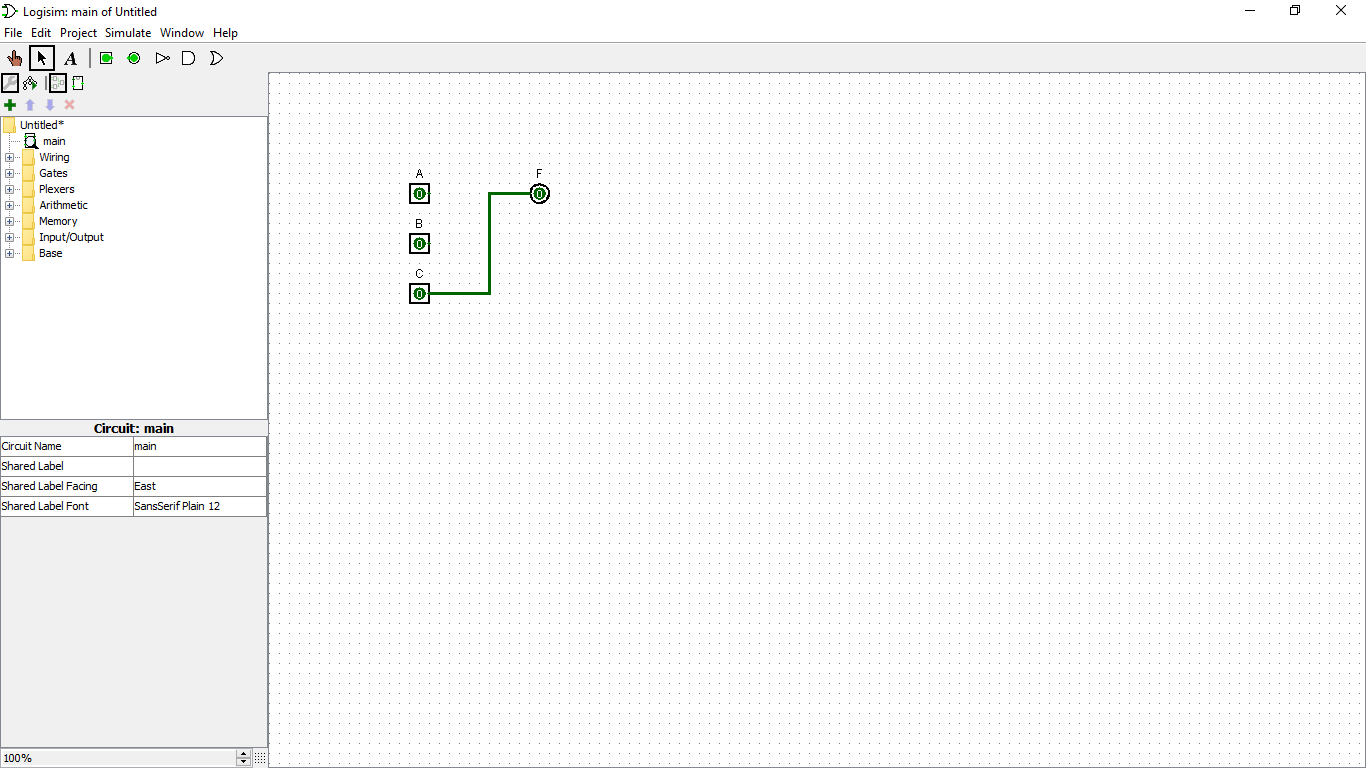
**Question 4: Problem 4.4 (b) 3-input, 1-output circuit, output is 1 when binary value of inputs is odd**

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | F |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A\BC | 00 | 01 | 11 | 10 |
| 0 | 0 0 | 1 1 | 1 3 | 0 2 |
| 1 | 0 4 | 1 5 | 1 7 | 0 6 |

F(A,B,C)=C

F(A,B,C)=∑m(1,3,5,7)



**Question 5: Problem 4.16 Carry propagate: Pi=Ai+Bi, carry generate: Gi=AiBi  
Show that the output carry and output sum of FA becomes:  
  
Ci+1=(Ci’Gi’+Pi’)’  
Si=(PiGi’) XOR Ci**

(Ci’Gi’+Pi’)’  
=(Ci+Gi)Pi=GiPi+PiCi  
=AiBi(Ai+Bi)+(Ai+ Bi)Ci  
=AiAiBi+AiBiBi+AiCi+BiCi  
=AiBi+AiCi+BiCi=Ci+1

(PiGi’) XOR Ci   
=(Ai+Bi)(AiBi)’ XOR Ci  
=(Ai+Bi)(Ai’Bi’) XOR Ci   
=(Ai’Bi+AiBi’) XOR Ci  
=Ai XOR Bi XOR Ci  
=Si

Output of NOR gate connected to A0 and B0= (A0+ B0)’  
= P0’

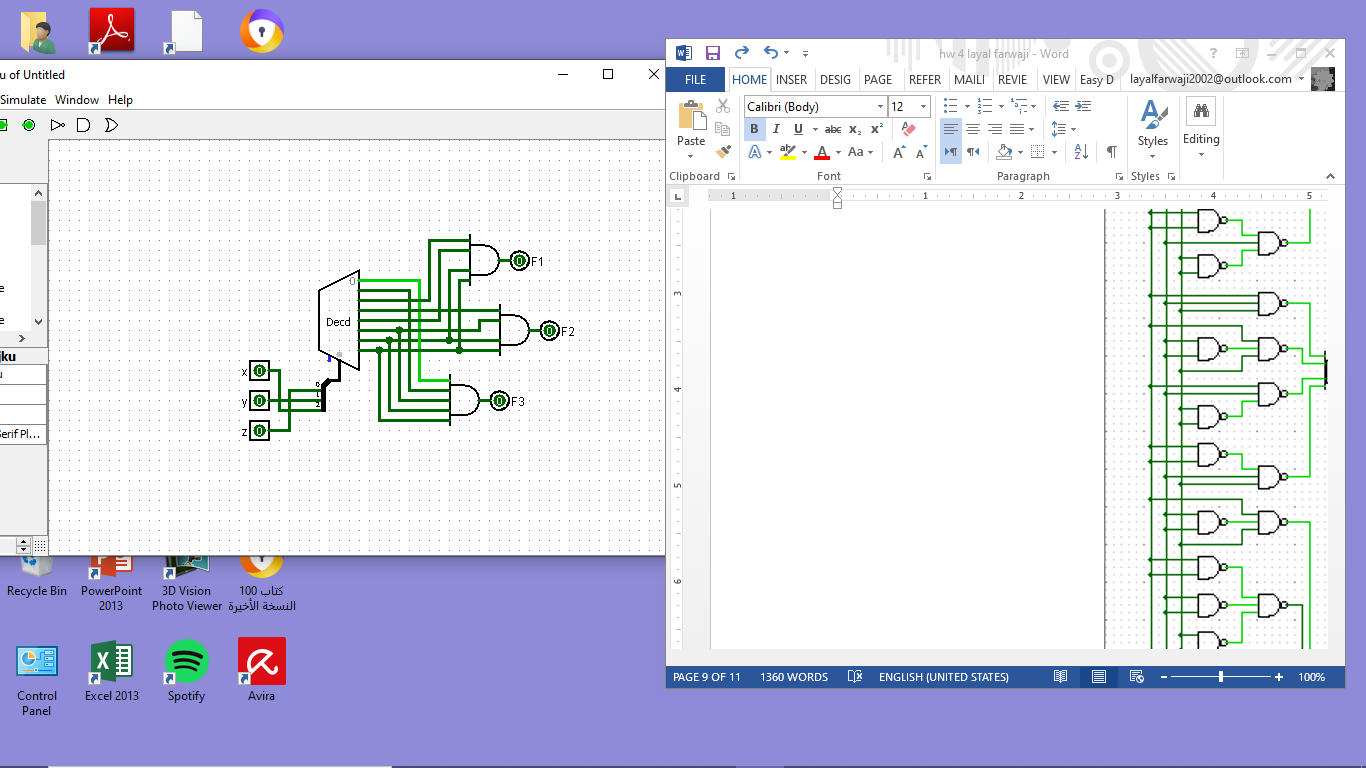
Output of NAND gate connected to A0 and B0= (A0B0)’  
= G0’

S0= (P0G0’) XOR C0

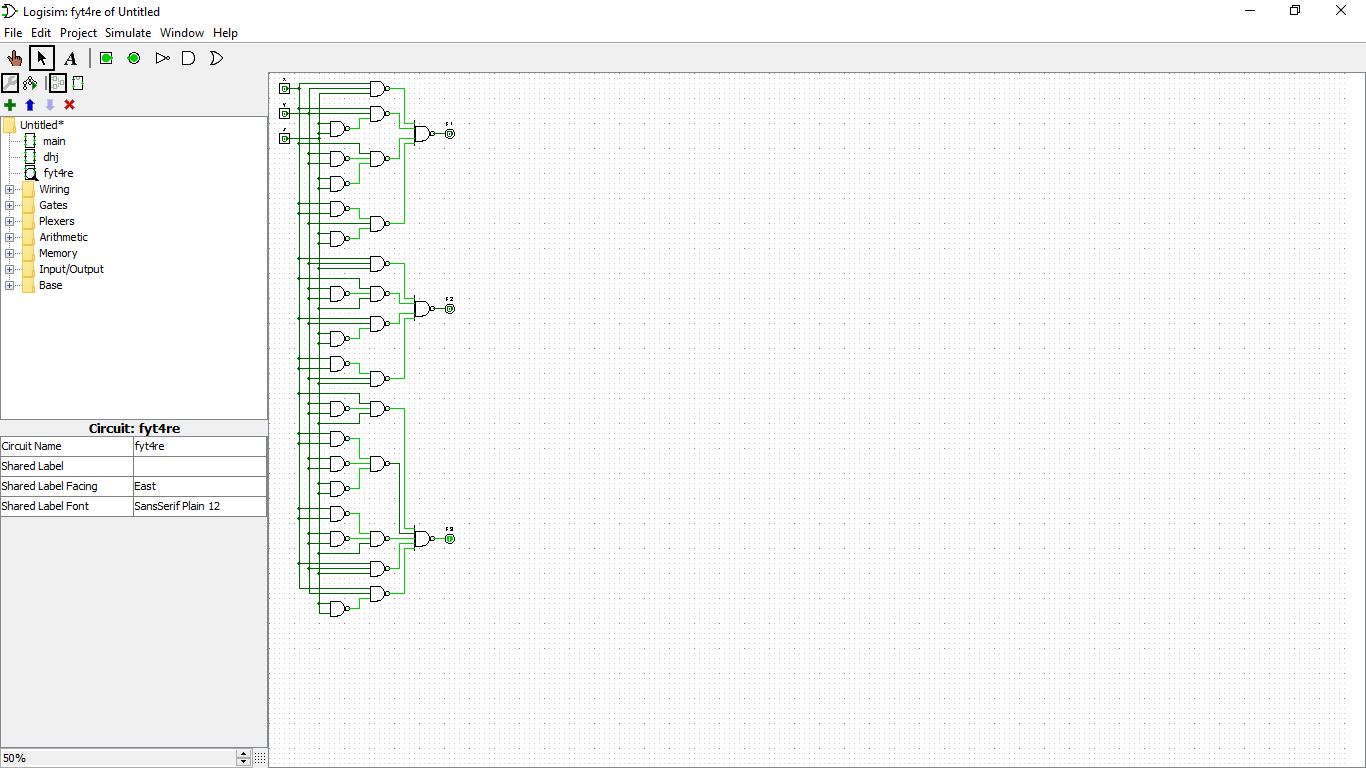
C1= (C0’G0’+P0’)’ as defined, so circuit implements full adder circuit

**Question 6: Problem 4.28 (a) Design decoder circuit constructed with NAND gates**

1. **F1=xy+xz’+yz’**

**F2=xz+xy+yz  
F3=y’z+x’y’z’+xy**

F1=xy(z+z’)+xz’(y+y’)+yz’(x+x’)  
=xyz+xyz’+xyz’+xy’z’+xyz’+x’yz’  
=xyz+xyz’+xy’z’+x’yz’  
=∑m(2,4,6,7)

F2=xz(y+y’)+xy(z+z’)+yz(x+x’)  
=xyz+xy’z+xyz+xyz’+xyz+x’yz  
=xyz+xy’z+xyz’+x’yz  
=∑m(3,5,6,7)

F3=y’z(x+x’)+x’y’z’+xy(z+z’)  
=xy’z+x’y’z+x’y’z’+xyz+xyz’  
=∑m(0,1,5,6,7)

**Question 7: Problem 4.32 (a) Implement function with multiplexer**

1. **F(A,B,C,D)=(0,2,5,8,10,14)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 0 | 0 1 | 0 3 | 1 2 |
| 01 | 0 4 | 1 5 | 0 7 | 0 6 |
| 11 | 0 12 | 0 13 | 0 15 | 1 14 |
| 10 | 1 8 | 0 9 | 0 11 | 1 10 |

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Y |
| 0 | 0 | D’ |
| 0 | 1 | C’D |
| 1 | 0 | D’ |
| 1 | 1 | CD’ |

I0  
I1 Y  
I2  
I3  
 S1 S0

D’  
C’D  
D’  
CD’

A B

4:1 MUX

**Question 8: Problem 4.33 Implement full subtractor with two 4:1 multiplexers**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Bin | D | Bout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

K-map for D:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A\B Bin | 00 | 01 | 11 | 10 |
| 0 | 0 0 | 1 1 | 0 3 | 1 2 |
| 1 | 1 4 | 0 5 | 1 7 | 0 6 |

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Y |
| 0 | 0 | A |
| 0 | 1 | A’ |
| 1 | 0 | A’ |
| 1 | 1 | A |

K-map for Bout:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A\B Bin | 00 | 01 | 11 | 10 |
| 0 | 0 0 | 1 1 | 1 3 | 1 2 |
| 1 | 0 4 | 0 5 | 1 7 | 0 6 |

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Y |
| 0 | 0 | 0 |
| 0 | 1 | A’ |
| 1 | 0 | A’ |
| 1 | 1 | 1 |

I0  
I1 Y  
I2  
I3  
 S1 S0

A  
A’  
A’  
A

B Bin

4:1 MUX

D

I0  
I1 Y  
I2  
I3  
 S1 S0

0  
A’  
A’  
1

B Bin

4:1 MUX

Bout